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Applicant(s): Rajagopalan et al.

Serial No.: 09/465,131

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For: METHOD AND APPARATUS FOR THERMAL PROFILING OF FLIP-CHIP PACKAGES

Art Unit: 2859

Examiner: Guadalupe, Yaritza

CERTIFICATE OF MAILING

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October 7, 2002 Pamela M. Stone
Date Pamela M. Stone

APPEAL BRIEF UNDER 37 C.F.R. § 1.192

Box AF
Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Appellant submits this appeal brief under 37 C.F.R. § 1.192 appealing the rejection of Claims 1-6 in Paper No. 12.

(1) Real Party in Interest

The real party in interest in the subject application is LSI Logic Corporation.

(2) Related Appeals and Interferences

No related appeals or interferences are known to appellant.

(3) Status of Claims

Claim 7 was canceled in Amendment "A" mailed on May 8, 2001.

Claims 8-11 were canceled in Amendment "A" subject to the restriction requirement.

Claims 1-6 are pending in the subject application.

Claims 1, 4 and 5 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art (APA) in view of U.S. Patent 6,321,175 to Nagaraj (*Nagaraj*).

Claims 2 and 3 stand finally rejected under 35 USC §103(a) as being unpatentable over admitted prior art in view of *Nagaraj* as applied to Claims 1, 4 and 5 and further in view of U.S. Patent No. 5,681,757 to Hayes (*Hayes*).

Claim 6 stands finally rejected under 35 USC §103(a) as being unpatentable over admitted prior art in view of *Nagaraj* and further in view of U.S. Patent No. 5,585,577 to Lemoine (*Lemoine*).

(4) Status of Amendments

The amendments filed on May 8, 2001 (Amendment "A"),

September 6, 2001 (Amendment "B"), October 24, 2001 (Amendment "C"), and May 1, 2002 (Amendment "D") have been entered.

(5) Summary of Invention

The present invention provides a thermal profiling device for accurately measuring the temperature at the interface between a semiconductor die and a packaging substrate of an integrated circuit during a reflow process in which the die is attached to the substrate. In one aspect of the present invention, a thermal profiling device for a flip-chip integrated circuit includes a packaging substrate of a flip-chip integrated circuit; a semiconductor die of the flip-chip integrated circuit having an active circuit surface for interconnecting the semiconductor die to the packaging substrate wherein the active circuit surface is secured to an upper surface of the packaging substrate; and a thermocouple secured directly to the active circuit surface of the semiconductor die for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process.

(6) Issues on Appeal

The following issues are on appeal:

Issue 1: Whether *Nagaraj* teaches securing a thermal sensor directly to the active circuit surface of a semiconductor die as recited in Claim 1;

Issue 2: Whether motivation exists in the cited prior art for modifying *Nagaraj* to arrive at the claimed invention; and

Issue 3: Whether the modification proposed by the rejection arrives at the claimed invention.

(7) Grouping of Claims

A statement that the claims of a group do not stand or fall together is not included with this appeal brief.

(8) Argument

Nagaraj does not teach securing a thermal sensor directly to the active circuit surface of a semiconductor die

Claim 1 recites a thermocouple secured directly to the active circuit surface of the semiconductor die for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process.

In section 2 of Paper No. 12, the rejection argues that *Nagaraj* discloses locating a thermal sensor (20) on the top side (18) of a printed circuit board (10) at column 4, lines 28-30, and concludes that locating the thermal sensor (20) on the top side (18) of the printed circuit board (10) "as best understood by the Examiner is directly mounted on the active circuit surface of the die/printed circuit board".

The rejection errs in confusing the top side (18) of the printed circuit board (10) in FIG. 5 of *Nagaraj* with the claimed active circuit surface of a semiconductor die by the device of combining the two terms "die" and "printed circuit board" with a slash. The rejection relies on selecting one structure from the reference and another structure from the claim and combining the two with a slash to imply that they are equivalent. However, the rejection clearly recognizes

that the claimed active circuit surface of a semiconductor die is not equivalent to the substrate to which the die is attached by arguing that "APA discloses the substrate and semiconductor die secured in place by a solder bond between the bumps and the bonding pads, securing the thermocouple in position. APA does not disclose the thermocouple secured directly to the active circuit surface of the semiconductor die as stated in Claim 1". The rejection contradicts itself by recognizing the structural distinction between the claimed active circuit surface of a semiconductor die and a substrate to which the die is attached while at the same time alleging that the printed circuit board in *Nagaraj* is structurally equivalent to the claimed active circuit surface of a semiconductor die, even though their structural differences are well known to one of ordinary skill in the art and even though their structural differences may readily be appreciated from FIGS. 2 and 5 of *Nagaraj*.

Nagaraj discloses the top side (18) of the printed circuit board (10) to which a system controller integrated circuit (25) is attached. The system controller integrated circuit (25) may include a semiconductor die, however the active circuit surface of the semiconductor die would be completely enclosed by the package of the system controller integrated circuit (25) according to the figures and accompanying text in *Nagaraj*. Clearly the top side (18) of the printed circuit board (10) to which the system controller integrated circuit (25) is attached and the active circuit surface of the semiconductor die inside the system controller integrated circuit (25) are not equivalent.

Moreover, *Nagaraj* clearly does not teach securing the thermal sensor (20) directly to the active circuit surface of the die inside the system controller integrated circuit

(25) as alleged by the rejection. To the contrary, *Nagaraj* discloses locating the thermal sensor (20) outside the system controller integrated circuit (25) on a top or bottom surface of the printed circuit board (10) as shown in FIGS. 2 and 5. FIGS. 2 and 5 clearly show that the top or bottom surface of the printed circuit board (10) is not the active circuit surface of the semiconductor die inside the integrated circuit package of the system controller integrated circuit (25), therefore there is no basis in fact for concluding that locating the thermal sensor (20) on the top side (18) of the printed circuit board (10) teaches or suggests securing the claimed thermocouple directly to the active circuit surface of the semiconductor die inside the integrated circuit package of the system controller integrated circuit (25). Because locating the thermal sensor (20) on either the top or the bottom surface of the printed circuit board (10) as taught in *Nagaraj* does not meet the claimed limitation of a thermocouple secured directly to the active circuit surface of the semiconductor die, the allegation that *Nagaraj* teaches securing the thermal sensor (20) directly to the active circuit surface of a semiconductor die is false.

In contrast to securing the thermocouple directly to the active circuit surface of the die of the system controller integrated circuit (25), *Nagaraj* teaches locating the thermal sensor (20) on either side of the printed circuit board (10). If the thermal sensor (20) is mounted on the bottom side (19) of the printed circuit board (10), then the printed circuit board (10) separates the die of the system controller integrated circuit (25) from the thermal sensor (20), therefore the thermal sensor (20) cannot be secured directly to the active circuit surface of the die of the system controller integrated circuit (25). The rejection proposes

the alternative of locating the thermocouple on the top side (18) of the printed circuit board (10) as taught by *Nagaraj* and alleges that this arrangement arrives at the claimed invention. However, the location *Nagaraj* suggests on the top side (18) of the printed circuit board (10) is clearly not the active circuit surface of the die of the system controller (25). Moreover, *Nagaraj* teaches in column 4, lines 28-30 that locating the thermal sensor (20) on the top side (18) of the printed circuit board (10) results in at least some loss of measurement accuracy compared to the preferred location of the thermal sensor (20) on the bottom side (19) of the printed circuit board (10). The loss of accuracy taught by *Nagaraj* resulting from locating the thermal sensor (20) on the top side (18) of the printed circuit board (10) teaches away from the improved accuracy that would result from locating the thermal sensor (20) directly on the active circuit surface of the die of the system controller (25).

Because the top side (18) of the printed circuit board (10) disclosed in *Nagaraj* is not equivalent to the active circuit surface of the die of the system controller (25), *Nagaraj* does not teach or suggest the claimed securing of a thermocouple directly to the active circuit surface of a semiconductor die as alleged by the rejection.

<u>No motivation exists in the cited prior art for modifying *Nagaraj* to arrive at the claimed invention</u>

The rejection further errs in alleging that motivation exists in the cited prior art to make the proposed modification. Specifically, the rejection alleges in section 2 of Paper No. 12 that the motivation for making the proposed modification is "to avoid damages due to over heating/over

cooling that may affect the overall quality of the circuit". However, *Nagaraj* anticipates the problem of overheating and teaches a solution to the problem in column 2, lines 54-59 as follows:

> "According to the present invention, a single thermal sensing device may be employed to detect the thermal characteristics of two integrated circuit devices, and thereby allow a thermal sensing system to provide instruction to counteract an 'overheat' condition for one or both devices."

Because *Nagaraj* already anticipates the problem of overheating and provides a method of counteracting the problem, the problem of overheating alleged by the rejection to support the proposed modification does not exist in *Nagaraj*. Because the problem relied on by the rejection to provide motivation for making the proposed modification does not exist in *Nagaraj*, the motivation for making the proposed modification does not exist in *Nagaraj*.

Even if the modification proposed by the rejection would arrive at the claimed invention, and even if the problem of overheating did exist in *Nagaraj* to provide the motivation for making the modification proposed by the rejection, the loss of accuracy cited by *Nagaraj* in locating the thermal sensor (20) on the top side (18) of the printed circuit board (10) is motivation <u>not</u> to make the proposed modification.

Specifically, *Nagaraj* teaches in column 4, lines 19-30, that the arrangement proposed by the rejection of locating the thermal sensor (20) on the top side (18) of the printed circuit board (10) results in a loss of accuracy compared to locating the thermal sensor (20) on the bottom side of the

printed circuit board (10) as illustrated in the preferred embodiment of FIG. 5:

> "It should be noted that the ambient temperature sensing capability for exemplary thermal sensor 20 is more accurate when closely coupled to the ground connection of the device to be measured. Thus, the placement of the thermal sensor 20 on the bottom side 19 of the printed circuit board 10 facilitates the accurate temperature measurement of system controller 25, which, in this example, has its ground interconnections located in the center portion of the device (see FIGS. 4 and 5). If the ground interconnections were located on the perimeter of the device, thermal sensor 20 could be located, for example, on the top side 18 of the printed circuit board 10 without excessive loss of measurement accuracy."

Because *Nagaraj* teaches that locating the thermal sensor (20) on the top side (18) of the printed circuit board (10) results in a loss of accuracy in measuring the temperature of the integrated circuit device (25), *Nagaraj* clearly teaches away from locating the thermal sensor (20) on the top side (18) of the printed circuit board (10) with respect to his intended purpose of achieving accurate temperature measurements. Because *Nagaraj* teaches away from locating the thermal sensor (20) on the top side (18) of the printed circuit board (10) with respect to his intended purpose of achieving accurate temperature measurements, there is no motivation in *Nagaraj* to make the modification proposed by the rejection.

The rejection further errs in section 6 of Paper No. 12 by alleging that the loss of measurement accuracy from

locating the thermal sensor (20) on the top side (18) of the printed circuit board (10) taught by *Nagaraj* is an advantage. The loss of measurement accuracy admitted by *Nagaraj* is clearly not an advantage, rather a disadvantage, which is precisely why *Nagaraj* teaches away from locating the thermal sensor (20) on the top side (18) of the printed circuit board (10). The loss of measurement accuracy cited in *Nagaraj* is further evidence that the top side (18) of the printed circuit board (10) is not the claimed active circuit surface of the claimed semiconductor die as alleged by the rejection.

Not only are the structural differences between the claimed invention and *Nagaraj* clearly evident to one of ordinary skill in the art as explained above, but also the examiner is not entitled to ignore the functional language in determining patentability as implied in section 6 of Paper No. 12. Functional limitations are explained in MPEP § 2173.05(g) as follows:

> "A functional limitation is an attempt to define something by what it does, rather than by what it is (e.g., as evidenced by its specific structure or specific ingredients). There is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in and of itself, render a claim improper. *In re Swinehart*, 439 F.2d 210, 169 USPQ 226 (CCPA 1971).
>
> A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context which it is used. A functional limitation is often used in association with an element, ingredient, or step of a process to define a

> particular capability or purpose that is served by the recited element, ingredient, or step. ...
> It was held that the limitation used to define a radical on a chemical compound as 'incapable of forming a dye with said oxidizing developing agent' although functional, was perfectly acceptable because it set definite boundaries on the patent protection sought. *In re Barr*, 444 F.2d 588, 170 USPQ 33 (CCPA 1971)."

The rejection errs in failing to consider the claim limitation of measuring a temperature of the active circuit surface of the semiconductor die during a reflow process in determining patentability of Claims 1-6 under 35 U.S.C. § 103(a) as explained at MPEP § 2143.03:

> "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). 'All words in a claim must be considered in judging the patentability of that claim against the prior art.' *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)."

Specifically, *Nagaraj* is directed to monitoring the temperature of an operating integrated circuit (25)(see column 4, lines 8-17, and FIGS. 4 and 5), which changes more slowly over time and over a smaller temperature range as compared to the temperature of the active circuit surface of a semiconductor die during a reflow process. Because the temperature changes are much more rapid during a reflow process than in the operation of an integrated circuit, the location of the thermocouple is much more critical to the

accuracy of the temperature measurements in a reflow process than in applications that monitor slower and smaller variations in temperature, such as the operation of an integrated circuit disclosed in *Nagaraj*. Because the location of the thermocouple is less critical in *Nagaraj* than in the claimed reflow process, *Nagaraj* would realize no apparent benefit from the modification proposed by the rejection, even if motivation could be found for making such a modification, and even if the proposed modification would arrive at the claimed invention. Because *Nagaraj* would realize no apparent benefit from the modification proposed by the rejection, there is no motivation to make the modification proposed by the rejection.

Because *Nagaraj* teaches away from making the proposed modification and because *Nagaraj* would realize no apparent benefit from the modification proposed by the rejection with respect to *Nagaraj*'s intended purpose, there is no motivation to make the modification proposed by the rejection. Because no motivation exists in *Nagaraj* to make the proposed modification, the rejection of Claims 1, 4 and 5 fails to meet the criteria required for a rejection of obviousness under 35 U.S.C. § 103.

<u>The modification proposed by the rejection fails to arrive at the claimed invention</u>

As explained above, *Nagaraj* does not teach or suggest the claimed thermocouple secured directly to the active circuit surface of a semiconductor die because the active circuit surface of a semiconductor die is not equivalent to the top side of a printed circuit board as alleged by the rejection. Because the rejection proposes

securing the thermocouple to the top side of a printed circuit board as taught in *Nagaraj*, the rejection fails to arrive at the claimed invention.

Further, because the semiconductor die of the system controller integrated circuit (25) in *Nagaraj* is evidently completely enclosed inside the integrated circuit package, it is not possible to mount the thermal sensor (20) directly on the active circuit surface of the die of the system controller integrated circuit (25) simply by "providing" a thermocouple as proposed by the rejection. The rejection therefore errs in failing to explain how the proposed modification might be made by one of ordinary skill in the art.

Because the rejection of Claims 2, 3 and 6 relies on the same errors made in the rejection of Claims 1, 4 and 5, Claims 1-6 are not obvious under 35 U.S.C. § 103.

Conclusion

In summary, the rejection of Claims 1-6 is based upon a proposed modification of *Nagaraj* which does not arrive at the claimed invention and which cannot be performed in the manner proposed by the rejection. Further, no reasonable motivation for making the proposed modification has been shown to exist in *Nagaraj*. Because the proposed modification does not arrive at the claimed invention, because the proposed modification cannot be made as proposed by the rejection, and because no motivation has been established for making the proposed modification, Claims 1-6 are non-obvious under 35 U.S.C. § 103 over *Nagaraj*.

Respectfully submitted,

Eric James Whitesell
Reg. No. 38,657

Address all correspondence to:
FITCH, EVEN, TABIN & FLANNERY
120 So. LaSalle Street, Suite 1600
Chicago, Illinois 60603

Direct telephone inquiries to:
Leo J. Peters
(408) 433-4578

APPENDIX

Claims

1. A thermal profiling device for a flip-chip integrated circuit comprising:

a packaging substrate of a flip-chip integrated circuit;

a semiconductor die of the flip-chip integrated circuit having an active circuit surface for interconnecting the semiconductor die to the packaging substrate wherein the active circuit surface is secured to an upper surface of the packaging substrate; and

a thermocouple secured directly to the active circuit surface of the semiconductor die for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process.

2. The thermal profiling device of Claim 1 wherein the thermocouple is secured using an adhesive.

3. The thermal profiling device of Claim 2 wherein the adhesive comprises an epoxy.

4. The thermal profiling device of Claim 1 wherein the active circuit surface has electrically conductive bumps formed thereon and the upper surface of the packaging substrate includes a plurality of bonding pads wherein the semiconductor die is positioned on the packaging substrate such that the electrically conductive bumps are in electrical contact with the plurality of bonding pads.

5. The thermal profiling device of Claim 4 wherein the packaging substrate and the semiconductor die are secured

in place by a solder bond between the electrically conductive bumps and the plurality of bonding pads.

6. A thermal profiling device for a flip-chip integrated circuit comprising:

a packaging substrate of a flip-chip integrated circuit having a first surface and a second opposite surface;

an opening passing through the second opposite surface and through the first surface of the packaging substrate;

a semiconductor die of the flip-chip integrated circuit having an active circuit surface for interconnecting the semiconductor die to the packaging substrate wherein the active circuit surface is secured to the first surface of the packaging substrate; and

a thermocouple secured directly to the active circuit surface of the semiconductor die through the opening for measuring a temperature of the active circuit surface of the semiconductor die during a reflow process.